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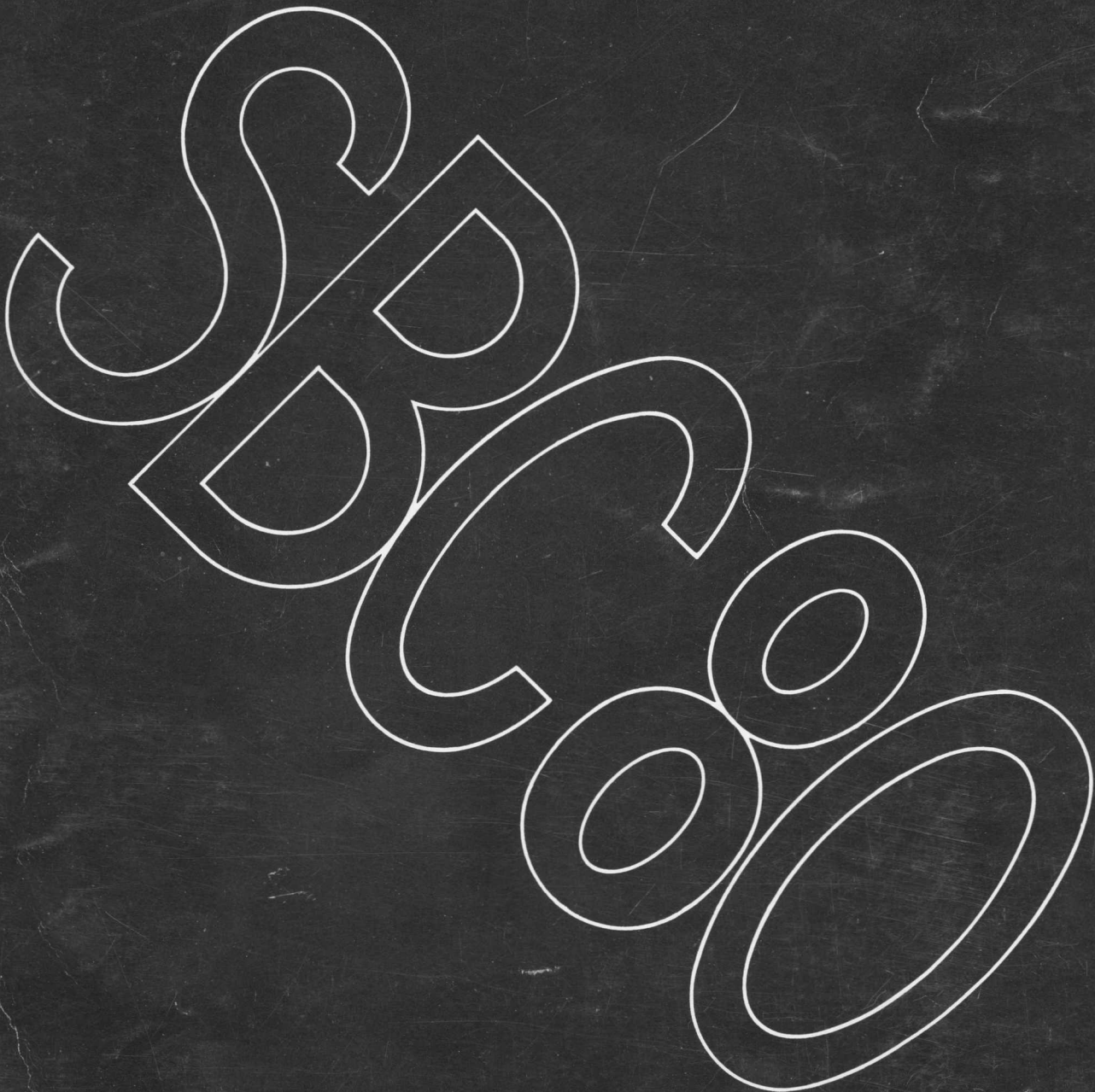
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**OEM COMPUTERS**

**SBC 508  
I/O EXPANSION BOARD  
HARDWARE REFERENCE MANUAL**



**\$500**

**SBC 508**  
**GENERAL PURPOSE INPUT/OUTPUT**  
**EXPANSION BOARD**  
**HARDWARE REFERENCE MANUAL**

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3065 Bowers Avenue  
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**SBC 508**

**HARDWARE REFERENCE MANUAL**

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The Input/Output (I/O) Expansion Board has been designed to increase the I/O capacity of any SBC 80 Single Board Computer. The I/O Expansion Board can also be used as part of the INTELLEC MDS Microcomputer Development System.

The I/O Expansion Board includes four input and four output ports. Each output port latches 8-bit data words and issues a framed strobe pulse, of selectable duration, to the device. All outputs are driven by TTL level buffer drivers. Each input port also supports 8 bits of data, latched or unlatched. All inputs are terminated by dual-in-line, socket-mounted resistor packs.

The I/O Board includes provisions for accepting eight external interrupt requests, buffering them and driving them on eight interrupt priority level lines. In addition, each of the eight I/O ports includes an interrupt request line that is activated by a strobe pulse from the device, then automatically cleared after the port is serviced. These port interrupt requests can be asserted on the system interrupt priority lines or can be used to feed an interrupt status port on this or another module. **WHEN USED IN CONJUNCTION WITH THE SBC 80/10, ONLY ONE INTERRUPT REQUEST LINE IS USED.**

The I/O Board accepts eight address inputs from the CPU. The two least significant address bits select one of the four input or output ports, while the six high-order address bits select the I/O Board. That is, these six high-order bits specify the BASE address of the I/O Board to be accessed. The user can select any one of 64 unique values for the BASE address (switch-selectable).

The I/O Board is implemented on a single, 12-in. X 6.75-in. printed circuit board. The board requires only +5 VDC power. Power and all system signals enter the board through an 86-pin, double-sided edge connector. An auxiliary 60-pin connector is available for use as a means of reaching vari-

ous test points. The module communicates with all peripheral devices via a 100-pin, double-sided edge connector, located on the top of the module, opposite the 86- and 60-pin connectors.

## 1. FUNCTIONAL DESCRIPTION OF THE I/O EXPANSION BOARD

The I/O Board can be divided into the following functional blocks:

- I/O address decode block
- Timing control block
- Input ports
- Output ports;

as shown in Figure 1.

The *I/O address decode block* determines when a particular I/O Board is being addressed, and then selects one of the four input or output ports to be accessed. An I/O Board is selected by the six most significant I/O address bits (the BASE address). The two least significant bits identify one of the four input or output ports. The BASE address is defined by positioning two nine-position rotary switches in the decode block. The six BASE address bits can provide 64 unique I/O Board select codes.

The *timing control block* provides user-selectable timing for the generation of the transfer acknowledge (XACK/) and output strobe (STBn/) signals. XACK/ acknowledges all input or output operations performed by the I/O Board. STBn/ (where n specifies one of the four ports, 0-3) strobes data, output through the I/O Board, into the proper external device. Timing for XACK/ and STBn/ is selected by connecting one of five jumper pairs in the timing control block.

The four *input ports* and four *output ports* provide a three-state buffered data path between the

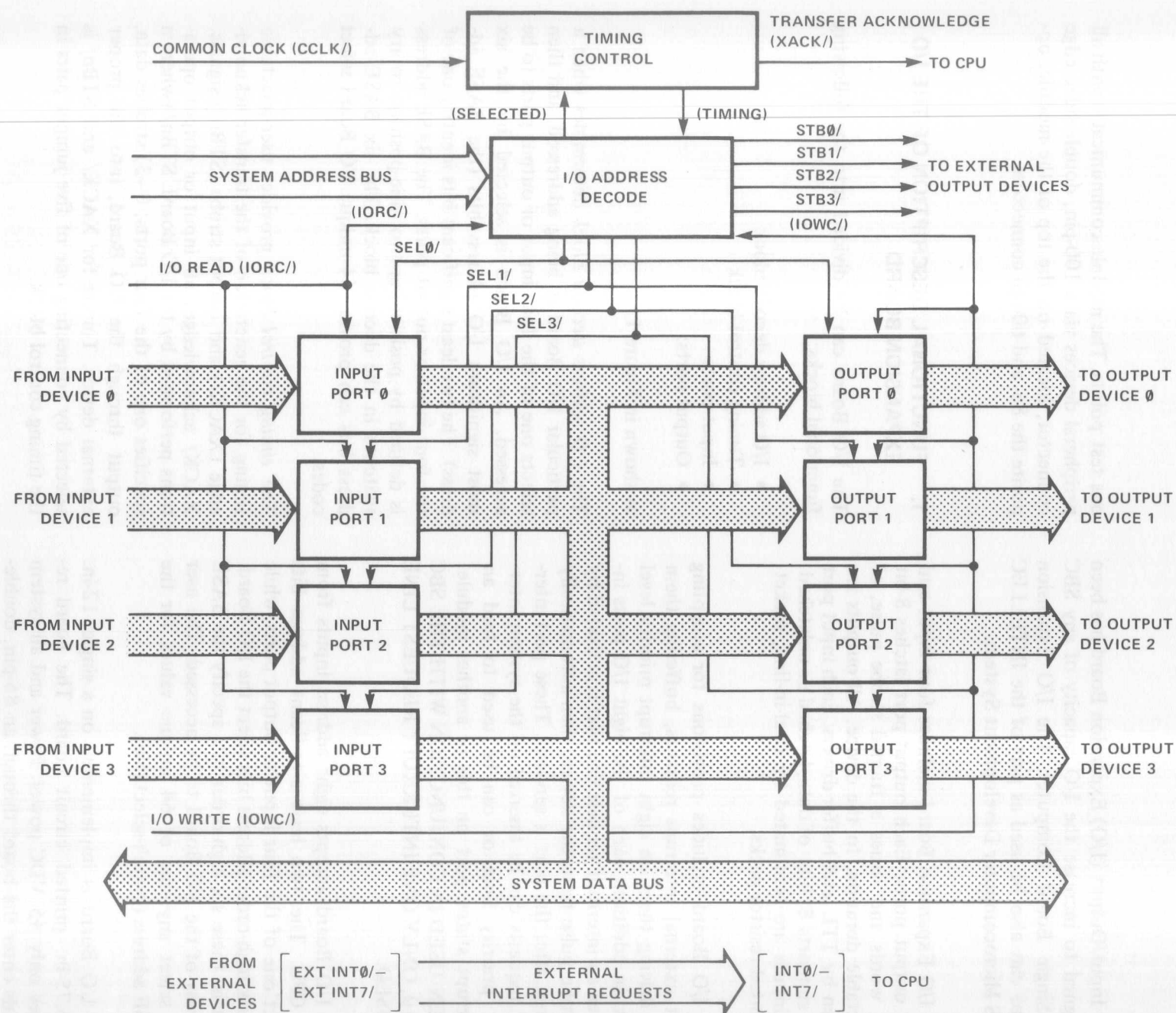


Figure 1. I/O Expansion Board Functional Block Diagram

system data bus and external devices. Each port is implemented with one of Intel's 8212 8-bit I/O port devices. Data can be latched or unlatched, and interrupt requests can be automatically set and reset by each 8212 device. In addition, each of the eight system interrupt lines can be driven by an external interrupt request line that can be activated by an external device.

## 2. EXPANSION BOARD: THEORY OF OPERATION

The following sub-sections provide a complete description of the theory of operation for each of the functional units of the I/O Board.

The I/O Board accepts/transmits signals, data and power through three different PC edge connectors:

- J1 Peripheral connector (to/from I/O peripherals)
- P1 Bus connector (to/from the system bus)
- P2 Auxiliary connector (to/from the auxiliary bus)

To avoid any ambiguity when referring to connector pins in subsequent paragraphs, we will always list the connector as well as the pin whenever such references are required; for example, P1-14 refers to pin 14 on connector P1. Pin lists for the three connectors are provided in Section 3.2.

The schematic (2 sheets) for the I/O Board is provided in Figure 6, located in Section 2.5.

### 2.1 I/O ADDRESS DECODE BLOCK

The I/O address decode block consists of three 3205 three-to-eight decoders, two nine-position rotary switches (for BASE address selection) and assorted gating circuits as shown on sheet 1 of the board schematic, Figure 6.

The two least significant address bits (ADR0/-ADR1/) feed the two least significant inputs (A0 and A1) on the first 3205 decoder (A14). This decoder is enabled by the outputs of the two rotary switches when the proper BASE address is recognized. The four least significant inverted out-

puts from this decoder define four select signals (SEL0/, SEL1/, SEL2/, SEL3/). Only one select signal will be true during an I/O cycle. Each SELn/ selects one of the four input and four output ports. The I/O read (IORC/) or write (IOWC/) command determines whether it is input port n or output port n which is selected by SELn/ (see Sections 2.2 and 2.3).

Each of the four outputs from the decoder also feed four 7402 negative-input AND gates. During output operations (i.e., when IOWC/ is true), the 7402 gate associated with the active SELn/ line is activated for a period determined by the timing control logic (see Section 2.2). The 7402 gates feed 7437 NAND gates which drive the output strobes (STB0/, STB1/, STB2/ and STB3/). STBn/ strobes the output data byte into the device interfaced to port n (see Section 2.2 for selectable timing of STBn/ signals).

The six most significant bits (ADR2/-ADR7/) of the 8-bit I/O address specify the BASE address of the I/O Board to be selected. Address lines ADR5/-ADR7/ are applied to the three address inputs of the second decoder (A24), while address lines ADR2/-ADR4/ are applied to the address inputs of the third decoder (A12). Both decoders are permanently enabled. The eight inverted outputs from each decoder feed one position on a nine-position rotary switch.

When ADR5/-ADR7/ specify a binary value equal to the setting of the X1 switch (S1), the output from S1 will be true. Similarly, when ADR2/-ADR4/ specify a binary value equal to the setting of the X2 switch (S2), the output from S2 will be true. The output from S1 and S2 must both be true to enable the port select decoder (A14), as previously mentioned. Note that setting either switch to position 9 disables the I/O Board. Table 1 correlates all possible combinations of switch settings with the 64 possible BASE addresses for the I/O Board.

### 2.2 TIMING

The timing control block consists of a 7474 D-type flip-flop, a 74161 synchronous 4-bit counter, a 7493 4-bit binary counter, a five-pair jumper pad for timing selection and various gating circuits, as

Table 1  
BASE ADDRESS SELECTION

BASE ADDRESS (HEX)	X1 SWITCH (S1)* SETTING	X2 SWITCH (S2)* SETTING	BASE ADDRESS (HEX)	X1 SWITCH (S1)* SETTING	X2 SWITCH (S2)* SETTING
00	1	1	80	5	1
04	1	2	84	5	2
08	1	3	88	5	3
0C	1	4	8C	5	4
10	1	5	90	5	5
14	1	6	94	5	6
18	1	7	98	5	7
1C	1	8	9C	5	8
20	2	1	A0	6	1
24	2	2	A4	6	2
28	2	3	A8	6	3
2C	2	4	AC	6	4
30	2	5	B0	6	5
34	2	6	B4	6	6
38	2	7	B8	6	7
3C	2	8	BC	6	8
40	3	1	C0	7	1
44	3	2	C4	7	2
48	3	3	C8	7	3
4C	3	4	CC	7	4
50	3	5	D0	7	5
54	3	6	D4	7	6
58	3	7	D8	7	7
5C	3	8	DC	7	8
60	4	1	E0	8	1
64	4	2	E4	8	2
68	4	3	E8	8	3
6C	4	4	EC	8	4
70	4	5	F0	8	5
74	4	6	F4	8	6
78	4	7	F8	8	7
7C	4	8	FC	8	8

\*Position 9 disables the I/O Module.

shown on sheet 1 of the board schematic, Figure 6.

The common clock pulse, CCLK/ (9.216 MHz), is inverted and applied to the A input of the 7493 counter. The QA output feeds the B input. Consequently, the QA output divides CCLK by 2, QB divides CCLK by 4, QC divides CCLK by 8 and QD divides CCLK by 16. That is, CCLK defines a 100-ns (approximately) period pulse, QA defines a 200-ns pulse, QB a 400-ns pulse, QC an 800-ns pulse and QD a 1600-ns pulse. Any one of these timing signals can be selected to drive the timing

control logic by connecting the proper jumper pair, as listed in Table 2.

The selected timing pulse ( $t_1$ ) feeds the clock input on the 74161 synchronous counter. This counter is cleared by the absence of either an I/O read (IORC/) or write (IOWC/) command. When IORC/ or IOWC/ goes true, however, the counter begins counting from zero. The QA output goes high with the first timing pulse and every other alternate pulse. When the QB output from the 74161 counter goes high (minimum= $t_1$ , maximum= $2t_1$ , after IORC/ or IOWC/ goes true), one of the output

Table 2  
TIMING SELECTION

TIMING PULSE ( $t_1$ ) (NANOSECONDS, NOMINAL)	JUMPER CONNECTION
100	1-2
200	3-4
400	5-6
800	7-8
1600	9-10

(Also refer to Figure 9-2)

strobe signals (STBn/) is enabled if IOWC/ is also true (i.e., if it is an output instruction), as mentioned in Section 2.1. QB remains high for two timing pulses ( $2t_1$ ). QC goes high as QB goes low. One  $t_1$  period later, QA goes high and clocks the high level on QC into the 7474 latch. The Q output

from the 7474 section causes the 74161 counter to be cleared. The  $\bar{Q}$  output feeds a 74125 circuit which drives XACK/ (via pin P1-23). XACK/ is enabled until IORC/ or IOWC/ goes false.

Figure 2 illustrates timing for the STBn/ and XACK/ signals.

## 2.3 INPUT OPERATIONS

The I/O Board includes four input ports, each implemented with an Intel 8212 device, as shown on sheet 2 of the module schematic, Figure 6. Figure 3 illustrates the logic within an 8212 device. In the input mode the MD input is held low (grounded).

If the data input by an external device is to be latched in the 8212 I/O port, or if an interrupt is to be generated when the data is input to the 8212, the device will accompany the input data byte with

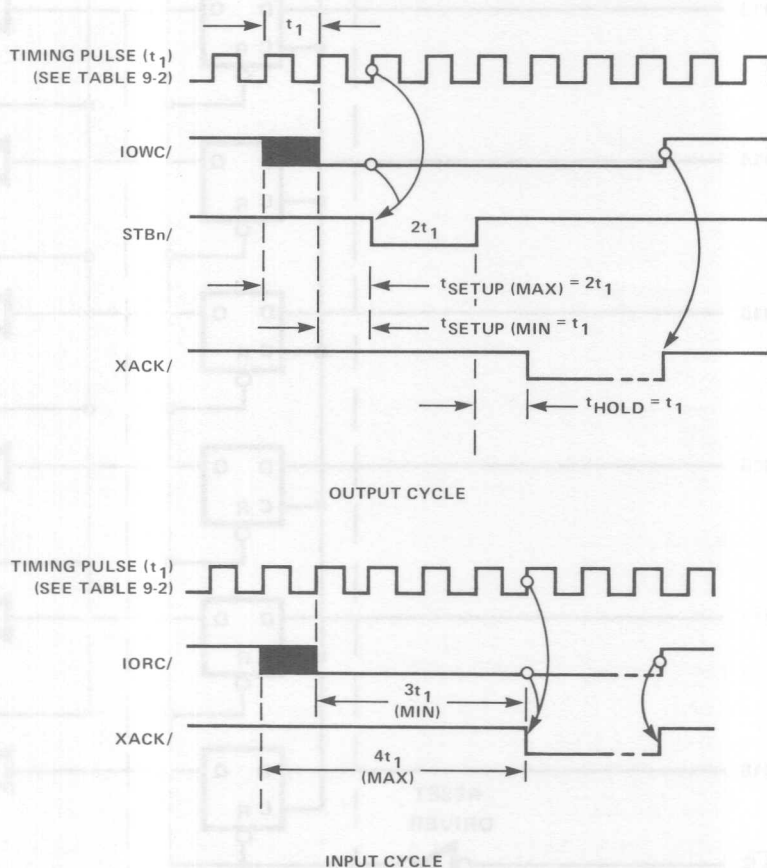


Figure 2. I/O Module Timing

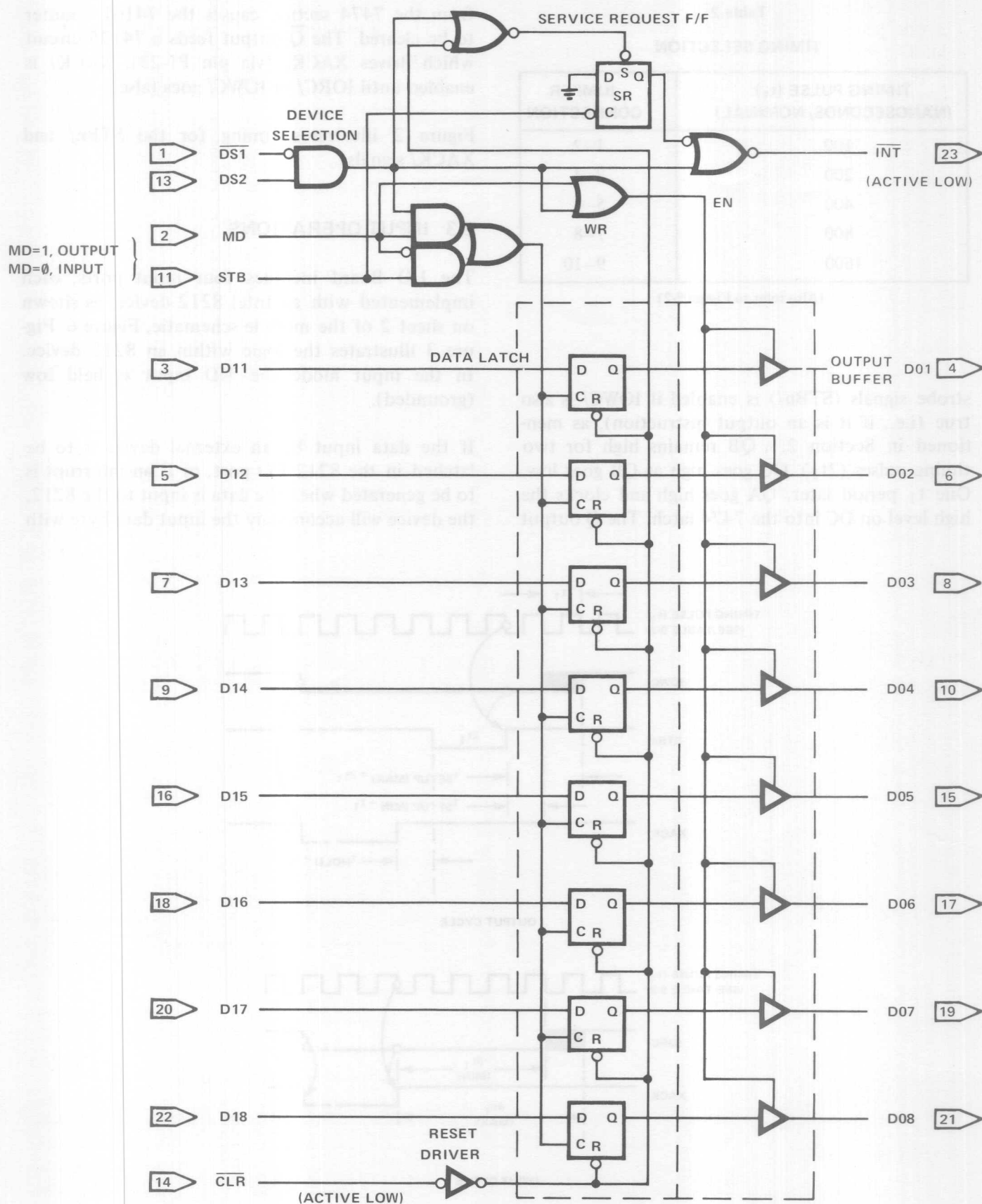


Figure 3. 8212 Logic Diagram

a strobe signal (ISTBn, where n is the port number). The data lines from the device are terminated by resistors provided by dual-in-line, socket-mounted resistor packs, and applied to the 8212. If ISTBn is present, the data will be latched in the 8212 when ISTBn goes low; the data will remain latched until ISTBn goes high again. If the strobe is not present, the output of a latch will always reflect the level on its input. In such a case, the data levels must be maintained by the device.

The negative-going edge of the strobe also clocks the service request flip-flop in the 8212, causing the interrupt request line (IINTn/) to go true (low). IINTn/ can be asserted on a system interrupt line or can be connected to one bit of an interrupt status register.

**NOTE:** Even if a strobe is not present, IINTn/ will be generated when the port is selected; consequently, IINTn/ should not be connected to the system interrupt input if interrupts are not desired.

When the CPU executes an I/O read instruction to a particular port, a select signal (SELn/) from the I/O address decode block enables the appropriate port as long as IORC is true. IORC (DS2) and SELn/ (DS1) enable the eight three-state output buffers within the 8212. These buffers drive the data on the system data bus (DAT0/-DAT7/).

The system reset signal (SYS RST) clears the latches and service request flip-flops in all of the 8212 I/O ports.

Figure 4 illustrates the timing within an input port.

In addition to the IINTn/ line from each 8212, an external device can always request an interrupt by pulling one of the eight external interrupt lines (EXINTm/) low (see sheet 1 of the module schematic), activating one of the INTm/ lines that are driven by 7407 non-inverting, open-collector buffers.

WHEN THE I/O EXPANSION BOARD IS CONNECTED TO THE SBC 80/10 AND IS INTERRUPT DRIVEN, THE I/O EXPANSION BOARD MUST USE INT1/ (PIN 42) OF THE SBC BUS AS THE INTERRUPT LEVEL BECAUSE THE SBC 80/10 ONLY ACCEPTS INTERRUPT LEVEL 1.

## 2.4 OUTPUT OPERATIONS

The I/O Module includes four output ports, each implemented with an Intel 8212 device, as shown on sheet 2 of the module schematic, Figure 6. Refer to Figure 3 for a logic diagram of the 8212. In the input mode, the MD input is held high.

When a peripheral device is ready to accept a data byte, it can request an interrupt by issuing an output strobe signal (OSTBn). OSTBn, from a device, is not to be confused with the output strobe signal (STBn/) that is sent to a device during an output cycle.

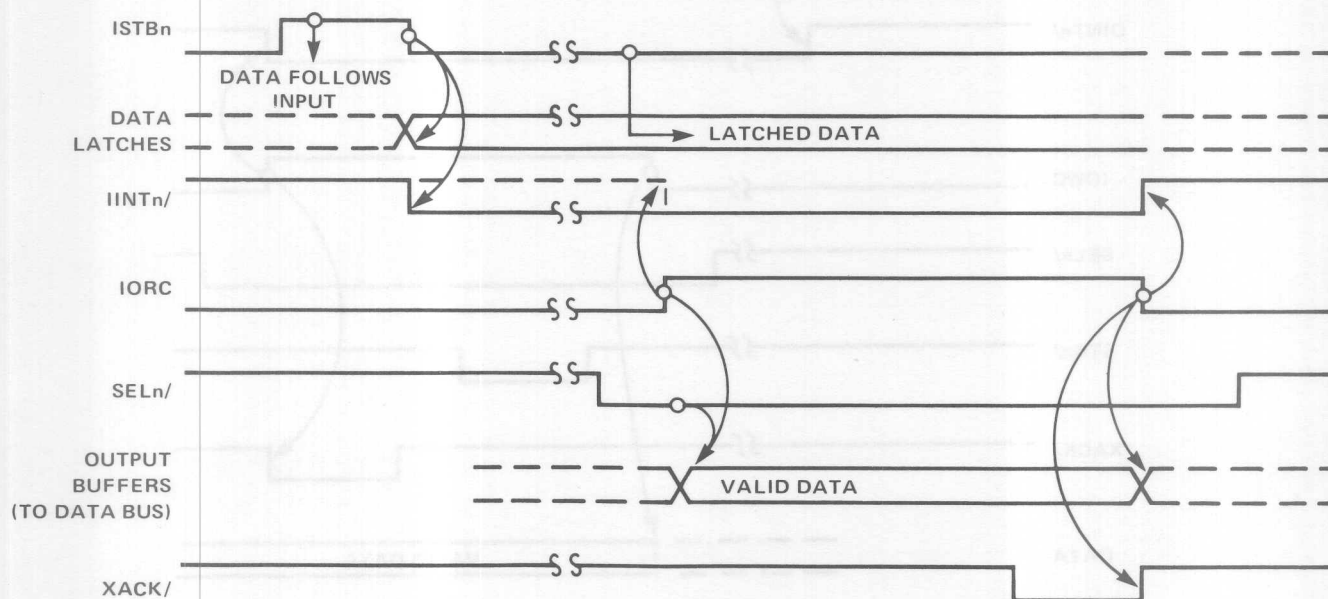


Figure 4. Input Port Timing

The service request flip-flop in the 8212 will be clocked on the negative-going edge of  $OSTB_n$ , causing the interrupt request signal for that device,  $OINT_n$ , to go true (low). The device can also request an interrupt by pulling one of the eight external interrupt lines ( $EXINT_m$ ) low. The primary difference between the two types of request is that the 8212's interrupt line ( $OINT_n$ ) is automatically cleared after the port is serviced, whereas the device is responsible for clearing its external interrupt line ( $EXINT_m$ ).

**NOTE:**  $OINT_n$ , like  $IINT_n$  on input ports, is generated when the port is selected, even if a strobe ( $OSTB_n$ ) was not issued by the device.

WHEN THE I/O EXPANSION BOARD IS CONNECTED TO THE SBC 80/10 AND IS INTERRUPT DRIVEN, THE I/O EXPANSION BOARD MUST USE  $INT1$  (PIN 42) OF THE SBC BUS AS THE INTERRUPT LEVEL BECAUSE THE SBC 80/10 ONLY ACCEPTS INTERRUPT LEVEL 1.

When the CPU executes an I/O write instruction to a particular port, a select signal ( $SEL_n$ ) from the I/O address decode block enables the appropriate port as long as  $IOWC$  is true. The output from the port latches will reflect the levels on the inputs (from the system data bus) until  $IOWC$  or  $SEL_n$  go false, at which time the data is latched. The 8212 output buffers are always enabled in the output

mode (i.e., when  $MD$  is high). The 7437 buffers drive data at active-low, TTL levels.

The system reset signal ( $SYS RST$ ) clears the latches and service request flip-flops in all of the 8212 I/O ports.  $SYS RST$  is also available to the external devices (pin J1-54) via a 74125 non-inverting buffer.

Figure 5 illustrates the timing within an output port.

## 2.5 I/O EXPANSION BOARD SCHEMATIC

Figure 6 provides a complete schematic drawing (2 sheets) of all logic on the I/O Board.

## 3. UTILIZATION: I/O EXPANSION BOARD

This section provides information on utilization of the I/O Board.

### 3.1 INSTALLATION

In installing the I/O Board, the user must take account of:

- environmental extremes
- mounting considerations
- electrical connections

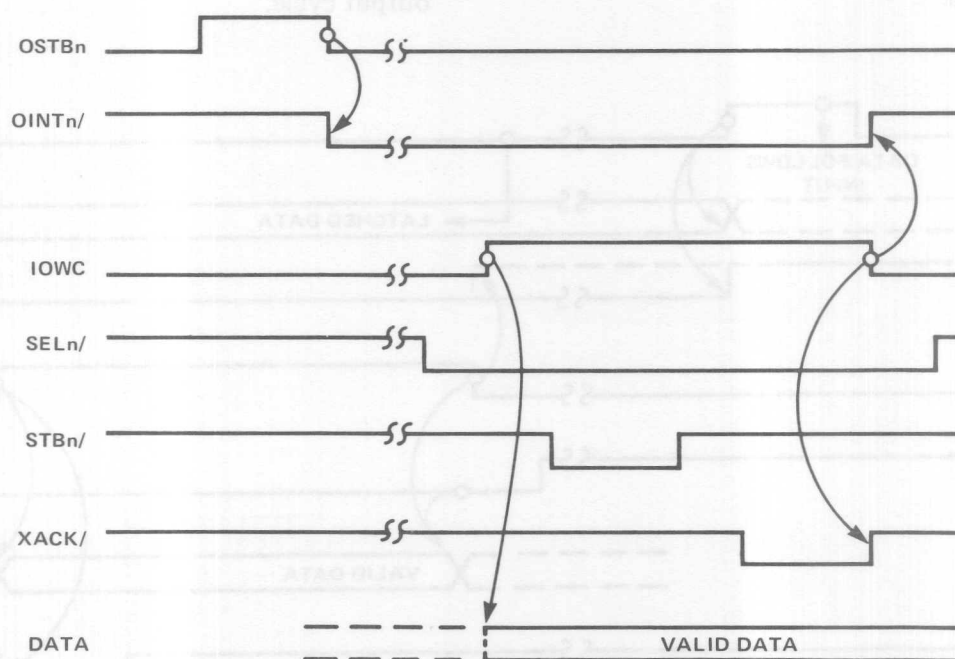
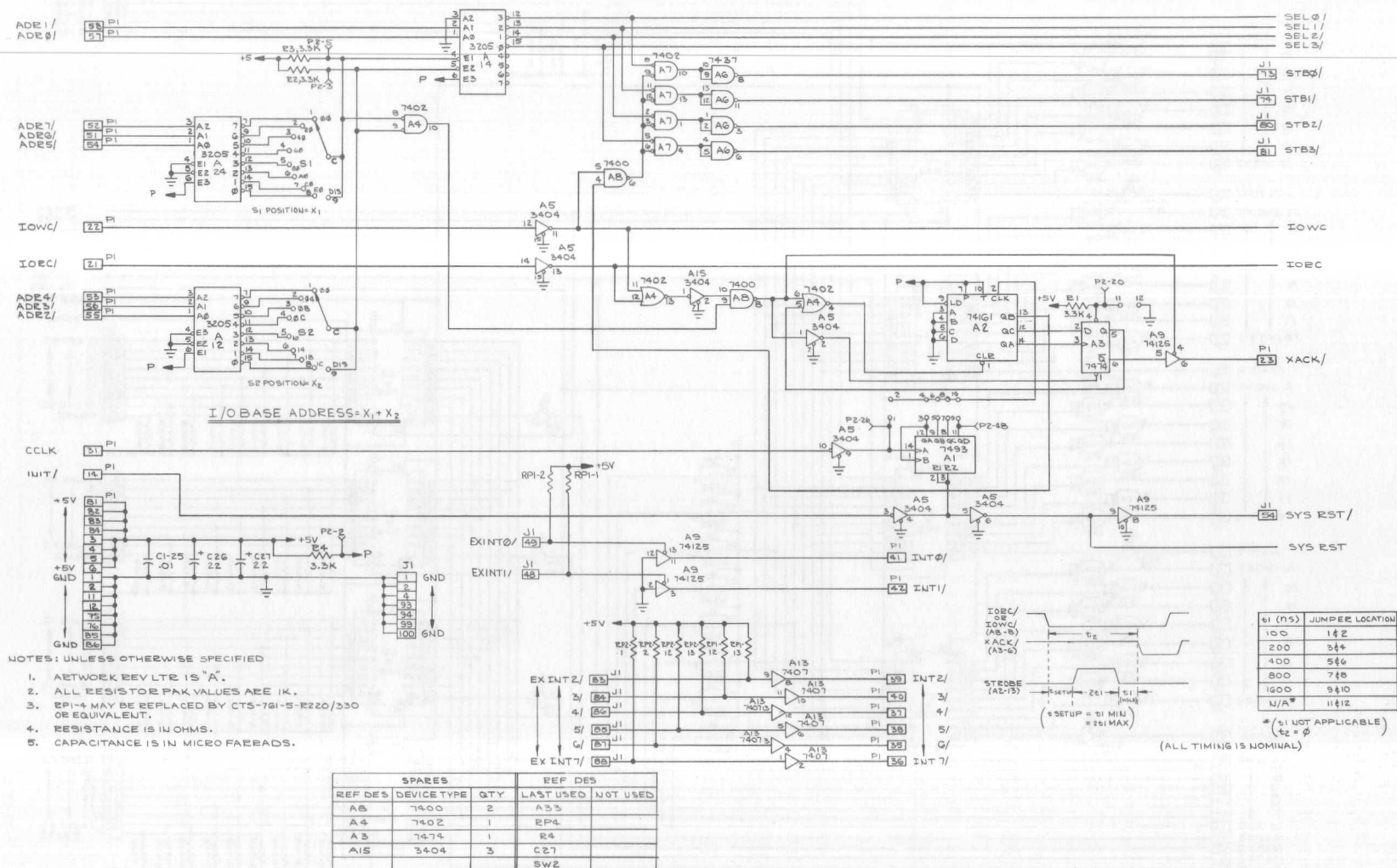


Figure 5. Output Port Timing



**Figure 6. I/O Board Schematic (Sheet 1 of 2)**

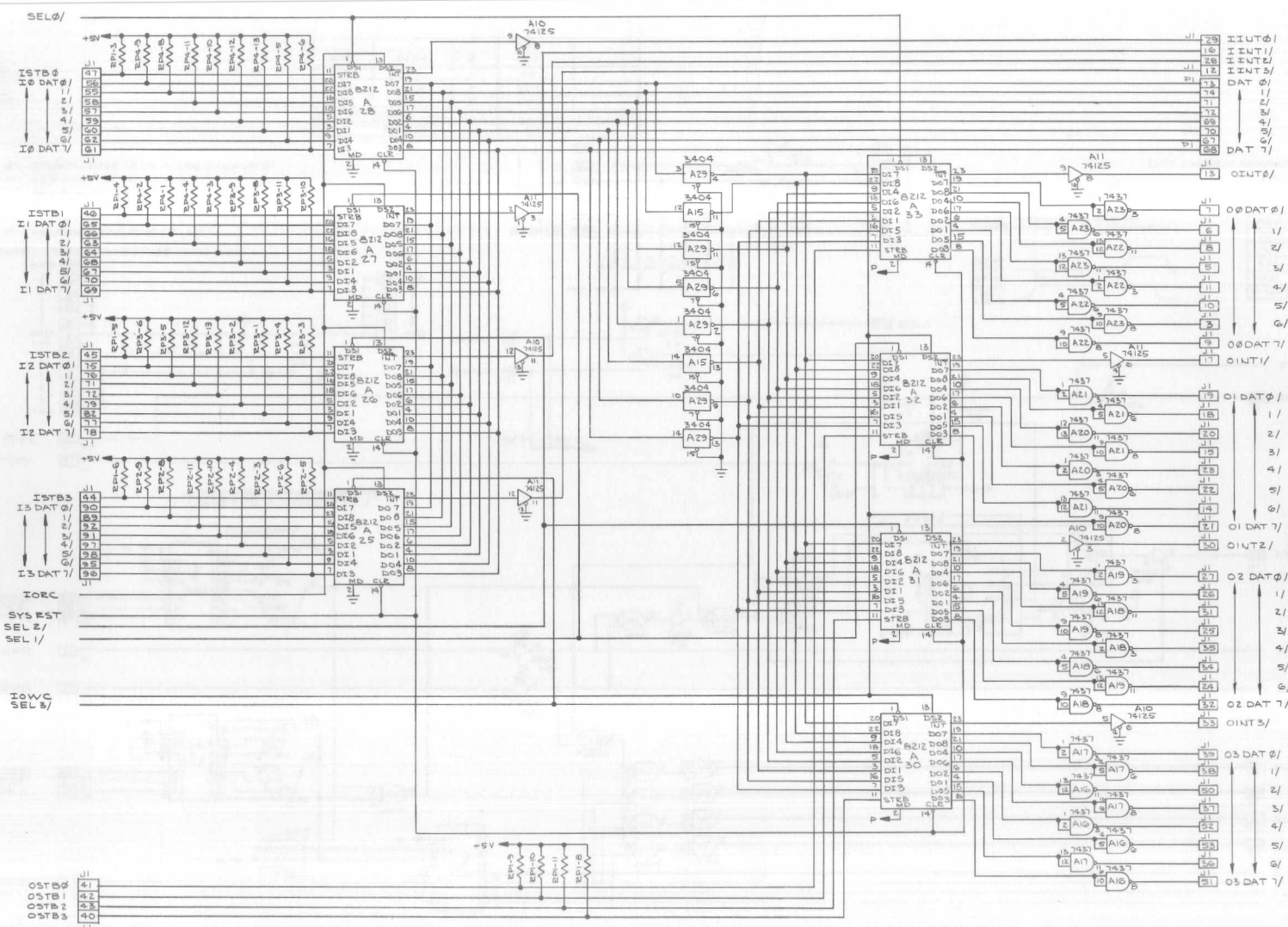


Figure 6. I/O Board Schematic (Sheet 2 of 2)

- (d) power requirements
- (e) signal requirements
- (f) base address selection
- (g) timing selection
- (h) bus termination packs

## Environment

Temperature extremes can cause instability, or result in permanent damage to the circuits on the board. Ambient temperature must therefore be maintained within the limits of 0° to 55° Centigrade. Exercise caution in locating the module, giving particular attention to radiant and conductive sources of heat. Remember that the board itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance, to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, non-condensing.

## Mounting

Avoid locating the module near vibrating machinery. Exposure to prolonged or violent vibration may cause fatigue or impact failure of connections on the board, resulting in abnormally high noise levels or outright failure of the assembly.

Dimensions of the board are 12-in. X 6.75-in. Be sure to allow enough additional clearance to ensure adequate cooling.

The board is designed to plug directly into the SBC 604 or SBC 614 Modular Cardcaged/Backplanes. The board may also be accessed via standard, double-sided PC edge connectors. An 86-pin connector and a 60-pin auxiliary connector are located on one edge of the board; a 100-pin connector is on the opposite edge. The connectors can serve as a mounting, as well as an electrical junction, if the environment is not too severe. Card guide slots are desirable, for the additional protection they afford. Should vibration be a problem, however, or should the assembly be used in a portable equipment application, an additional retaining bracket will have to be provided. When mounting the board, remember that it is desirable to orient the assembly vertically whenever possible. This optimizes convective cooling of the components on the board.

## Electrical Connections

The I/O Board communicates with the motherboard and, consequently, the rest of the system, through a standard 86-pin, double-sided PC edge connector (P1), 0.156-in. contact centers, as shown in Figure 9-7. Control Data VPB01E43A00A1 is one suitable type of connector. Pin allocations on this connector are given in Table 3 of Section 3.2. Test points are brought out through the auxiliary 60-pin, double-sided PC edge connector (P2), 0.1-in. contact centers (see Figure 7). Pin allocations for this connector are listed in Table 4. The module transfer information to/from the peripheral devices via a 100-pin, double-sided PC edge connector (J1) which attaches to the edge opposite that of the other two connectors. This connector has 0.1-in. contact centers. Viking 3VH50/1JN5 is one suitable type of connector for communicating with the peripheral devices. Pin allocations for this connector are given in Table 5.

The I/O Board requires only +5 VDC power.

$$V_{CC} = 5V \pm 5\%$$

$$I_{CC} = 2.5A \text{ max}$$

Refer to the pin list in Table 3 of Section 3.2 for power connections.

## Signal Requirements

All data and control functions appearing at the module edge connectors are at TTL levels. Electrical characteristics of the signal inputs and outputs, as well as power inputs are given in Section 4.

Signal descriptions and connector pin allocations are given in Section 3.2.

## Base Address Selection

The six most significant bits of the 8-bit I/O address define the BASE address for an I/O Board. The user must select a BASE address by positioning the X1 and X2 rotary switches as listed in Table 1. Notice that the I/O Board is disabled if either switch is in position 9.

## Timing Selection

The user must also select timing parameters for the generation of the output strobe (STBn/) and

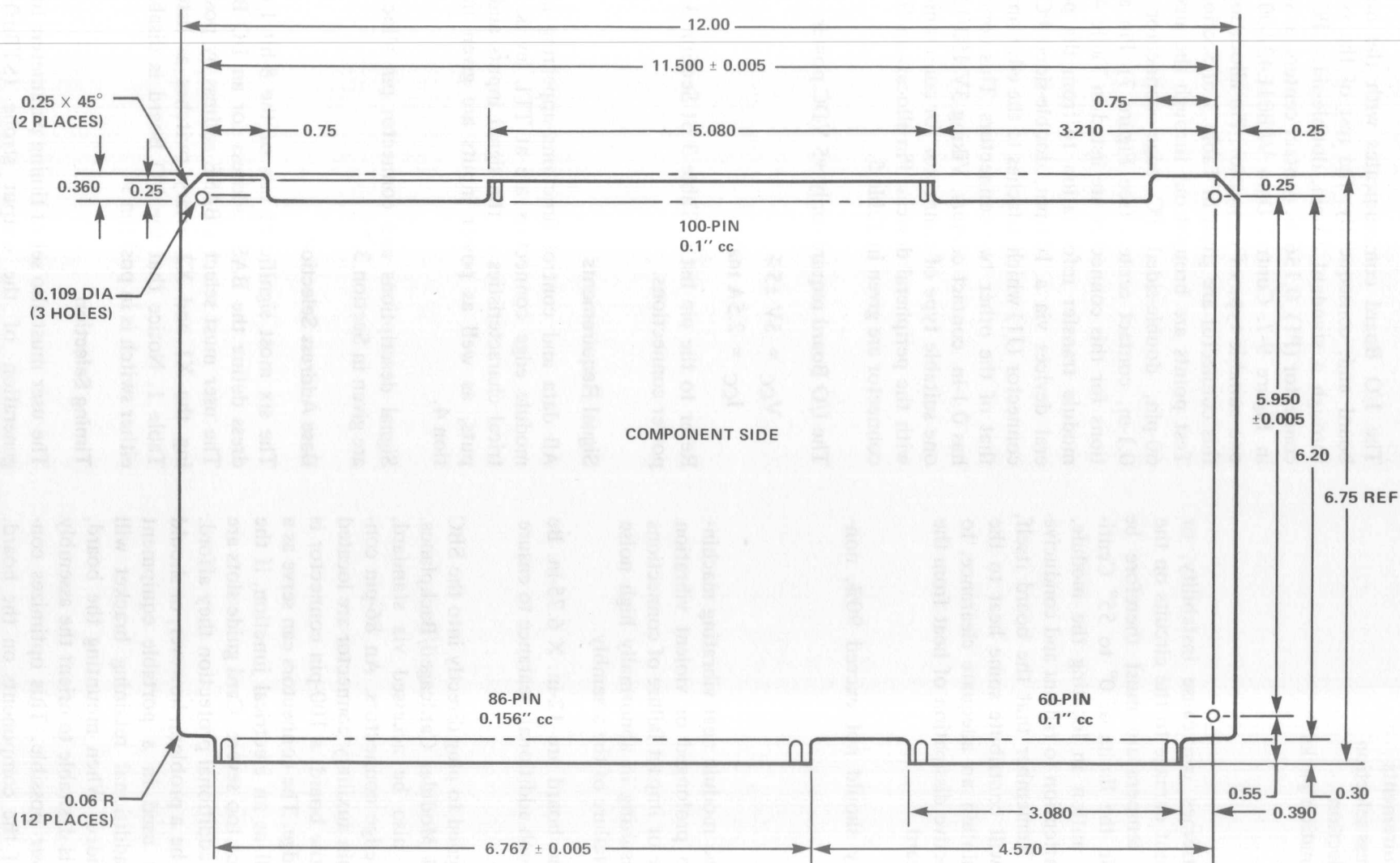


Figure 7. I/O Module Connectors

transfer acknowledge (XACK/) signals, that meet the timing requirements of the CPU and/or the external output devices being used. Specific timing is selected by connecting one of the five jumper pairs in the timing control block, as listed in Table 2. Figure 2 illustrates board timing relative to the timing pulse ( $t_1$ ) selected.

### Bus Termination Packs

The I/O Board includes provisions for installing dual-in-line, socket-mounted resistor packs for the purpose of terminating data lines from the external input devices (refer to sheet 2 of the board schematic). The user should install appropriate packs to match the drive characteristics of the external device with the DC characteristics of the 8212 data input lines.

### 3.2 PIN LISTS: I/O EXPANSION BOARD

The following section provides connector pin allocations on the I/O Board. The pins and their designated signal functions for the 86-pin connector

(P1) are listed in Table 3. The same information for the 60-pin auxiliary connector (P2) is listed in Table 4. Pin and signal information for the 100-pin peripheral connector (J1) is given in Table 5.

## 4. OPERATING CHARACTERISTICS: /IO EXPANSION BOARD

The AC and DC characteristics of all major signals that appear at the edge connectors will be listed in this section.

### 4.1 AC CHARACTERISTICS

AC characteristics are listed in Tables 6a and 6b.

### 4.2 DC CHARACTERISTICS

DC characteristics are listed in Tables 7a and 7b.

Table 3

## P1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION	PIN	SIGNAL	FUNCTION
1	GND	{ Ground	44	ADRF/	{ Address bus
2	GND		45	ADRC/	
3	+5 VDC	Power inputs	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7			50	ADR9/	
8			51	ADR6/	
9			52	ADR7/	
10			53	ADR4/	
11	GND	{ Ground	54	ADR5/	{ Address bus
12	GND		55	ADR2/	
13		System reset	56	ADR3/	
14	INIT/		57	ADRO/	
15			58	ADR1/	
16			59		
17			60		{ Data bus
18			61		
19			62		
20			63		
21	IORC/	I/O read command	64		
22	IOWC/	I/O write command	65		
23	XACK/	Acknowledge transfer	66		
24			67	DAT6/	
25			68	DAT7/	
26			69	DAT4/	
27			70	DAT5/	
28			71	DAT2/	
29			72	DAT3/	
30			73	DAT0/	
31	CCLK/	Common clock	74	DAT1/	
32			75	GND	{ Ground
33			76	GND	
34			77		{ Power inputs
35	INT6/	{ Interrupt requests	78		
36	INT7/		79		
37	INT4/		80		
38	INT5/		81	+5 VDC	
39	INT2/		82	+5 VDC	{ Power inputs
40	INT3/	{ Address bus	83	+5 VDC	
41	INT0/		84	+5 VDC	
42	INT1/		85	GND	{ Ground
43	ADRE/		86	GND	

Table 4

## P2 CONNECTOR PIN LIST TEST POINTS

PIN	SIGNAL	FUNCTION	PIN	SIGNAL	FUNCTION
1			31		
2		Pull-up	32		
3	X2 EN/	X2 Address Select	33		
4			34		
5	X1 EN/	X1 Address Select	35		
6			36		
7			37		
8			38		
9			39		
10			40		
11			41		
12			42		
13			43		
14			44		
15			45		
16			46		
17			47		
18			48		
19			49		
20	SET XACK/	XACK direct set	50		
21			51		
22			52		
23			53		
24			54		
25			55		
26	CCLK/	Common clock	56		
27			57		
28			58		
29			59		
30			60		

Table 5

## J1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	GND	{ Ground
2	GND	
3	O0DAT6/	{ Data out bus from port 0, but 6
4	GND	
5	O0DAT3/	{ Data out bus from output port 0
6	O0DAT1/	
7	O0DAT0/	
8	O0DAT2/	
9	O0DAT7/	
10	O0DAT5/	
11	O0DAT4/	
12	IINT3/	Interrupt from input port 3
13	OINT0/	Interrupt from output port 0
14	O1DAT6/	{ Data out bus from
15	O1DAT3/	
16	IINT1/	Interrupt from input port 1
17	OINT1/	Interrupt from output port 1
18	O1DAT1/	{ Data out bus
19	O1DAT0/	
20	O1DAT2/	
21	O1DAT7/	
22	O1DAT5/	
23	O1DAT4/	{ Data out bus
24	O2DAT6/	
25	O2DAT3/	
26	O2DAT1/	
27	O2DAT0/	
28	IINT2/	Interrupt from input port 2
29	IINT0/	Interrupt from input port 0
30	OINT2/	Interrupt from output port 2
31	O2DAT2/	{ Data out bus
32	O2DAT7/	
33	OINT3/	Interrupt from output port 3
34	O2DAT5/	{ Data out bus
35	O2DAT4/	
36	O3DAT6/	{ Data out bus
37	O3DAT3/	
38	O3DAT1/	
39	O3DAT0/	
40	OSTB3	{ Output strobes
41	OSTB0	
42	OSTB1	
43	OSTB2	
44	ISTB3	{ Input strobes
45	ISTB2	
46	ISTB1	
47	ISTB0	
48	EXTINT1/	{ External interrupt
49	EXTINT0/	
50	O3DAT2/	Data out bus from output port 3

**Table 5**  
**J1 CONNECTOR PIN LIST (continued)**

PIN	SIGNAL	FUNCTION
51	O3DAT7/	{ Data out bus from output port 3
52	O3DAT4/	
53	O3DAT5/	
54	SYS RST/	System reset
55	I0DAT1/	{ Data in bus to input port 0
56	I0DAT0/	
57	I0DAT3/	
58	I0DAT2/	
59	I0DAT4/	
60	I0DAT5/	
61	I0DAT7/	
62	I0DAT6/	{ Data in bus to input port 1
63	I1DAT2/	
64	I1DAT3/	
65	I1DAT0/	
66	I1DAT1/	
67	I1DAT5/	
68	I1DAT4/	
69	I1DAT7/	{ Data in bus to input port 2
70	I1DAT6/	
71	I2DAT2/	{ Data in bus to input port 2
72	I2DAT3/	
73	STB0/	{ Output strobes to devices
74	STB1/	
75	I2DAT0/	{ Data in bus to input port 2
76	I2DAT1/	
77	I2DAT6/	
78	I2DAT7/	
79	I2DAT4/	{ Output strobes to devices
80	STB2/	
81	STB3/	{ Data in bus to input port 2
82	I2DAT5/	
83	EXT INT2/	
84	EXT INT3/	
85	EXT INT5/	
86	EXT INT4/	{ External interrupt requests
87	EXT INT6/	
88	EXT INT7/	
89	I3DAT1/	
90	I3DAT0/	{ Data in bus to input port 3
91	I3DAT3/	
92	I3DAT2/	
93	GND	{ Ground
94	GND	
95	I3DAT6/	{ Data in bus to input port 3
96	I3DAT7/	
97	I3DAT4/	
98	I3DAT5/	
99	GND	{ Ground
100	GND	

**Table 6**  
**I/O BOARD AC CHARACTERISTICS**

PARAMETER	OVERALL (nsec)		DESCRIPTION	REMARKS																		
	MIN.	MAX.	INPUT REQUIREMENTS																			
t <sub>AS</sub>	49		Address Setup Time To Command																			
t <sub>AH</sub>	49		Address Hold Time From Command																			
t <sub>DS</sub>	44		Data Setup Time To Command, Write																			
t <sub>DHW</sub>	45		Data Hold Time From Command, Write																			
t <sub>SEP</sub>	100		Command Separation																			
t <sub>WC</sub>	t <sub>ACC</sub>		Command Width																			
t <sub>XKCO</sub>	0		Command Turn Off Delay From SACK/																			
t <sub>BCY</sub>	100		Bus Clock Cycle Time																			
t <sub>BW</sub>	25		Bus Clock Low and High Periods																			
t <sub>CCY</sub>	100		Com. Clock Cycle Time																			
t <sub>CW</sub>	25		Com. Clock Low and High Periods																			
OUTPUT LIMITS																						
t <sub>XKO</sub>		80	XACK/ Turn Off Delay																			
t <sub>DHR</sub>	6		Data Hold From Read Command																			
t <sub>ACC</sub>		79	XACK Delay From Command	Jumper Location 11 & 12																		
		5nt <sub>CCY</sub> + 179	XACK Delay From Command	<table><tr><th>Jumper Loc's</th><th>n</th><th>t<sub>CCY</sub></th></tr><tr><td>Holes 1-2</td><td>1</td><td>100 ns</td></tr><tr><td>Holes 3-4</td><td>2</td><td>100 ns</td></tr><tr><td>Holes 5-6</td><td>4</td><td>100 ns</td></tr><tr><td>Holes 7-8</td><td>8</td><td>100 ns</td></tr><tr><td>Holes 9-10</td><td>16</td><td>100 ns</td></tr></table>	Jumper Loc's	n	t <sub>CCY</sub>	Holes 1-2	1	100 ns	Holes 3-4	2	100 ns	Holes 5-6	4	100 ns	Holes 7-8	8	100 ns	Holes 9-10	16	100 ns
Jumper Loc's	n	t <sub>CCY</sub>																				
Holes 1-2	1	100 ns																				
Holes 3-4	2	100 ns																				
Holes 5-6	4	100 ns																				
Holes 7-8	8	100 ns																				
Holes 9-10	16	100 ns																				
		679	XACK Delay From Command																			
		1179	XACK Delay From Command																			
		1679	XACK Delay From Command																			
		2179	XACK Delay From Command																			
		2679	XACK Delay From Command																			
t <sub>XKD</sub>	-41		XACK DELAY FROM VAL RD DATA	Jumper Loc's 11 & 12																		
	5nt <sub>CCY</sub> - 33			SEE t <sub>ACC</sub> , above																		

**Table 6**  
**I/O BOARD AC CHARACTERISTICS**




PARAMETER	OVERALL (nsec)		DESCRIPTION OUTPUT LIMITS	REMARKS
	MIN.	MAX.		
tEDSO*	nt <sub>CCY</sub> -53	74 58 70 64 30	OxDATy/setup to STBx/strobe	For n, see Table .a t <sub>ACC</sub> REMARKS
tESTB*	2nt <sub>CCY</sub> -61		STBx/ STROBE WIDTH	
tEDHO*	nt <sub>CCY</sub> +28		Output Data Hold From STBX/ strobe	
tDODAT			IOWC/to valid OxDATy/	
tDSTBI			OSTBx/or ISTBx/ Delay to OINTx/or IINTx/	
tDINT			IOWC/or IORC/ Delay to OINTx/ or IINTx/	
tINTRST			IOWC/or IORC/ Delay to RST I,OINTx/	
tEXINT			EXINTx/Delay to INTx/	
INPUT REQUIREMENTS				
tSTB	25		OSTBx, ISTBx WIDTH	
tEDSSTB	15		IxDATy/setup to ISTBx/	
tEDHSTB	20		IxDATy/hold from ISTBx/	
tEDSR	0		IxDATy/setup to IORC/	
tEDHR	0		IxDATy/hold from IINTx/	


\*Not applicable for jumper position 11-12.


**Table 7**  
**I/O BOARD DC CHARACTERISTICS**

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	PARAMETER		
				MIN.	MAX.	UNITS
ADR $\emptyset$ / $\rightarrow$ ADR7, IOWC/, IORC/, CLK/, INIT/  XACK/	V <sub>IL</sub>	Input Low Voltage	V <sub>IL</sub> = 0.45 V V <sub>IH</sub> = 5.25 V	2.0	0.85	V
	V <sub>IH</sub>	Input High Voltage				V
	I <sub>IL</sub>	Input Current at V <sub>IL</sub>			-0.25	mA
	I <sub>IH</sub>	Input Current at V <sub>IH</sub>			10	$\mu$ A
	C <sub>L</sub>	Capacitive Load			15	pF
	V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 16 mA	2.4	0.4	V
	V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5.2 mA			V
	I <sub>LH</sub>	Output Leakage High	High Z V <sub>O</sub> = 2.4 V		40	$\mu$ A
	I <sub>LL</sub>	Output Leakage Low	High Z V <sub>O</sub> = 0.4 V		-40	$\mu$ A
	C <sub>L</sub>				15	pF
INT $\emptyset$ / $\rightarrow$ INT7/	V <sub>OL</sub>		I <sub>OL</sub> = 16 mA		0.4	V
	I <sub>OH</sub>		Output is OFF V <sub>OH</sub> = 5.5 V		250	$\mu$ A
	C <sub>L</sub>				15	pF
DAT $\emptyset$ $\rightarrow$ DAT7/	V <sub>OL</sub>		I <sub>OL</sub> = 15 mA		0.45	V
	V <sub>OH</sub>		I <sub>OH</sub> = -1 mA	3.65		V
+5V $\pm$ 5%	V <sub>IL</sub>			2.0	0.85	V
	V <sub>IH</sub>					V
	I <sub>IL</sub>				-0.35	mA
	I <sub>IH</sub>				110	$\mu$ A
	C <sub>L</sub>				15	pF
	I <sub>+5V</sub>	+5 Volts Supply Current			2.5	A

**Table 7**  
**I/O BOARD DC CHARACTERISTICS**

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	PARAMETERS		
				MIN.	MAX.	UNITS
STB $\emptyset$ / $\rightarrow$ STB3/ OxDATy/,  (x=0,1,2,3; y=0 $\rightarrow$ 7)	V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 48 mA		0.4	V
	V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1.2 mA	2.4		V
	C <sub>L</sub>	Capacitive Load			15	pF
OINTx/, IINTx/ (x=0,1,2,3), SYS RST/ IxDATy/, ISBx, OSTBx (x=0,1,2,3; y=0 $\rightarrow$ 7)	V <sub>OL</sub>		I <sub>OL</sub> = 16 mA		0.4	V
	V <sub>OH</sub>		I <sub>OH</sub> = -5.2 mA	2.4		V
	C <sub>L</sub>				15	pF
EXINT0/ $\rightarrow$ EXINT7/	V <sub>IL</sub>	Input Low Voltage			0.85	V
	V <sub>IH</sub>	Input High Voltage		2.0		V
	I <sub>IL</sub>	Input Current at V <sub>IL</sub>	V <sub>IL</sub> = 0.45 V 		-5.25	mA
	I <sub>IH</sub>	Input Current at V <sub>IH</sub>	V <sub>IH</sub> = 5.25 V 		260	$\mu$ A
	C <sub>L</sub>				15	pF
	V <sub>IL</sub>			2	0.8	V
	V <sub>IH</sub>					V
	I <sub>IL</sub>		V <sub>IL</sub> = 0.4 V 		-6.6	mA
	I <sub>IH</sub>		V <sub>IH</sub> = 2.4 V		40	$\mu$ A
	C <sub>L</sub>				15	pF

 Includes 5 mA due to a 1 K terminating resistor (this changes if the user changes resistor pack values).

 Includes 250  $\mu$ A due to 1 K terminating resistor (which changes if resistor pack is changed).

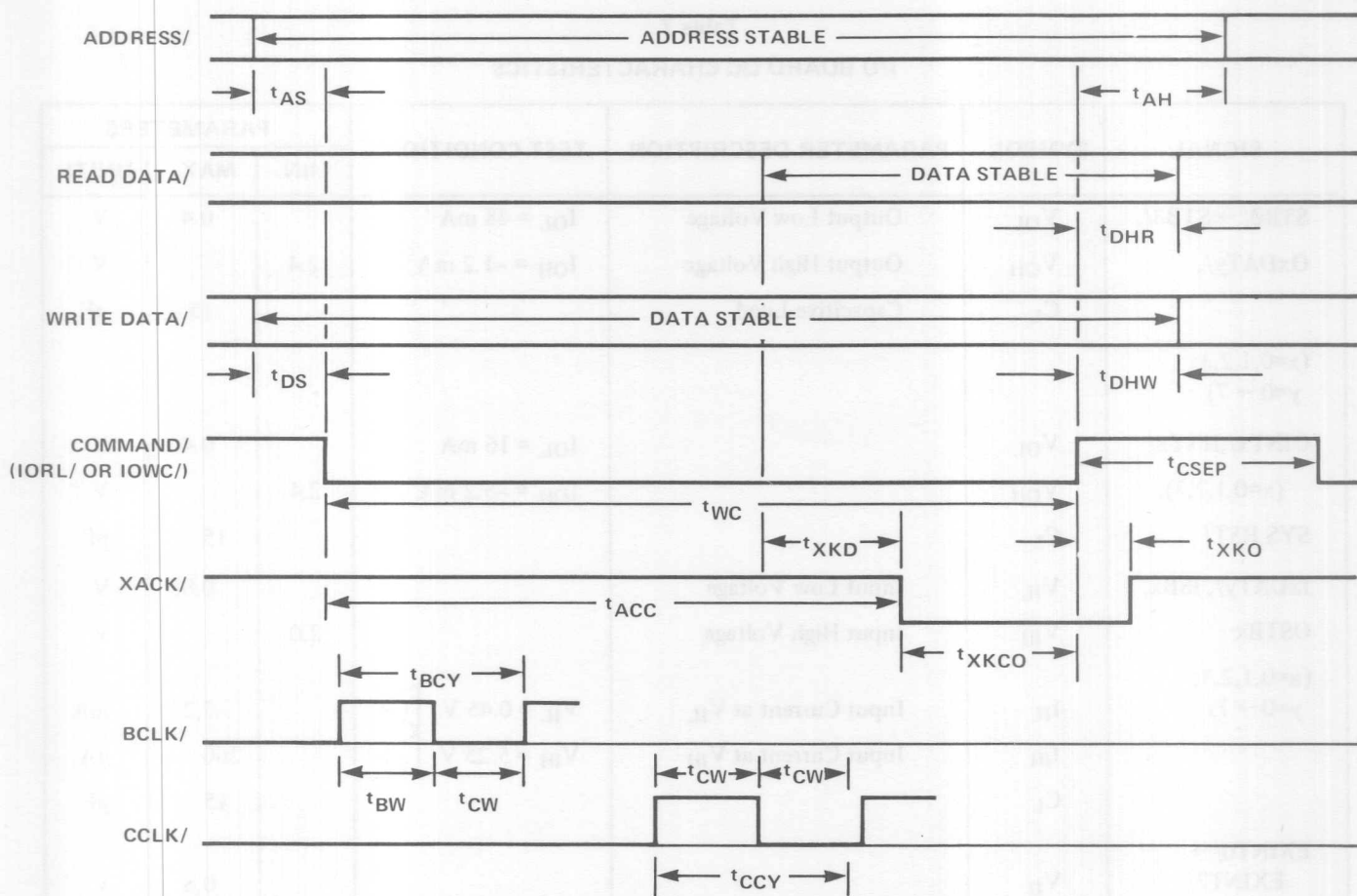


Figure 8. Command Timing

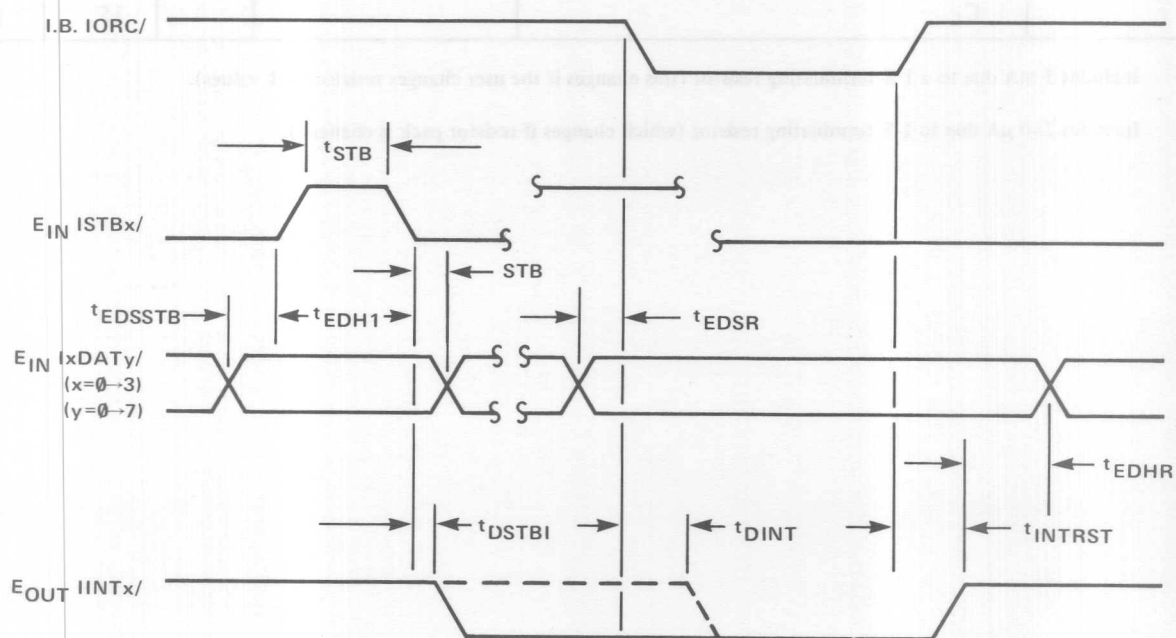


Figure 9a. External I/O Read Timing

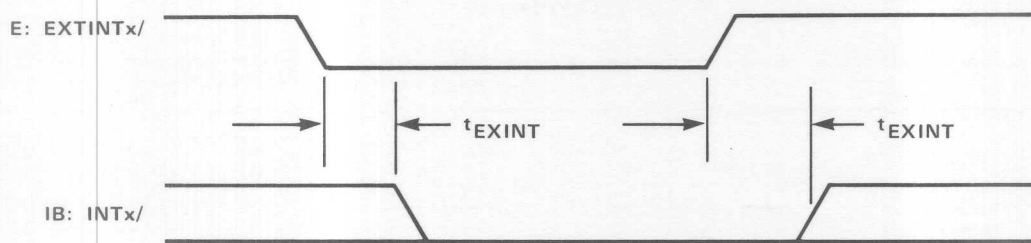


Figure 9b. Interrupt Timing

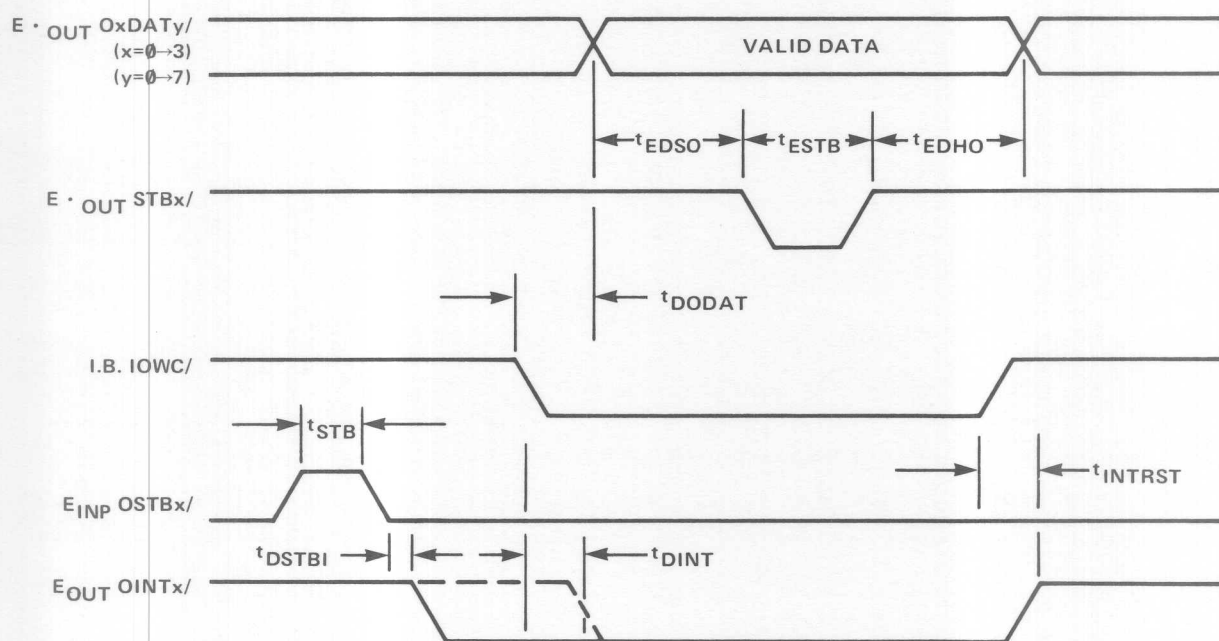


Figure 10. External I/O Write Timing

